Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method for increasing control information from a single general purpose input/output (GPIO) mechanism, the method comprising:

utilizing a single GPIO mechanism with a socket on a computer system; and

determining whether a first card, a second card, or no card is installed in the socket according to detected changes in signal states on a single signal line between the GPIO mechanism and the socket.

2. (Original) The method of claim 1 wherein determining further comprises writing a signal in a first state by a POST (power-on self test) routine to the GPIO mechanism.

3. (Original) The method of claim 2 wherein determining further comprises reading a state of the GPIO mechanism by the POST routine.

4. (Original) The method of claim 3 wherein determining further comprises writing the signal in a second state by the POST routine to the GPIO mechanism.

5. (Original) The method of claim 4 further comprising reading a state of the GPIO mechanism by the POST routine.

6. (Original) The method of claim 5 wherein when the state of the GPIO mechanism changes in accordance with state changes by the POST routine, no card is installed in the socket.

7. (Original) The method of claim 6 wherein when the state of the GPIO mechanism does not change, one of the first and second cards is installed.

8. (Original) The method of claim 7 wherein one of the first and second cards pulls-up the signal line, and the other of the first and second cards pulls-down the single signal line.

9. (Canceled)

10. (Previously Presented) A system for increasing control information from a single general purpose input/output (GPIO) mechanism, the system comprising:

a computer system planar including a socket; and

a GPIO means coupled to the socket via a single signal line, wherein at least three states of occupancy of the socket are detected according to state changes on the single signal line.

11. (Original) The system of claim 10 wherein when a first card occupies the socket, the single signal line is pulled to a first logic state.

12. (Original) The system of claim 11 wherein when a second card occupies the socket, the single signal line is pulled to a second logic state.

13. (Original) The system of claim 12 wherein when no card occupies the socket, the single signal line changes state in response to state changes of a signal from a POST (power-on self test) routine.

14. (Original) The system of claim 13 further comprising a controller coupled to the GPIO to perform the POST routine.

15. (Original) The system of claim 14 further comprising a transient storage circuit coupled to the single signal line to assist in the detection of state changes.

16. (Original) The system of claim 15 wherein the transient storage circuit comprises a resistor-capacitor (R-C) circuit.

17. (Original) A method to allow trinary state determination from a single signal line, the method comprising:

providing a GPIO (general purpose input/output) mechanism for a socket on a computer system planar; and

utilizing a transient storage circuit on a signal line between the GPIO mechanism and the socket to allow detection of at least three separate conditions of the socket.

18. (Original) The method of claim 17 wherein utilizing a transient storage circuit further comprises utilizing an R-C (resistor-capacitor) circuit.

19. (Original) The method of claim 18 wherein utilizing an R-C circuit further comprises detecting a first state on the signal line indicating presence of a first card in the socket, detecting a second state on the signal line indicating presence of a second card in the socket, and detecting a state change on the signal line indicating no card presence in the socket.

20. (Original) The method of claim 19 wherein detecting the first state, the second state, and the state change further comprises detecting whether state of the signal line changes in response to signals sent by a POST (power-on self test) routine to the GPIO mechanism.